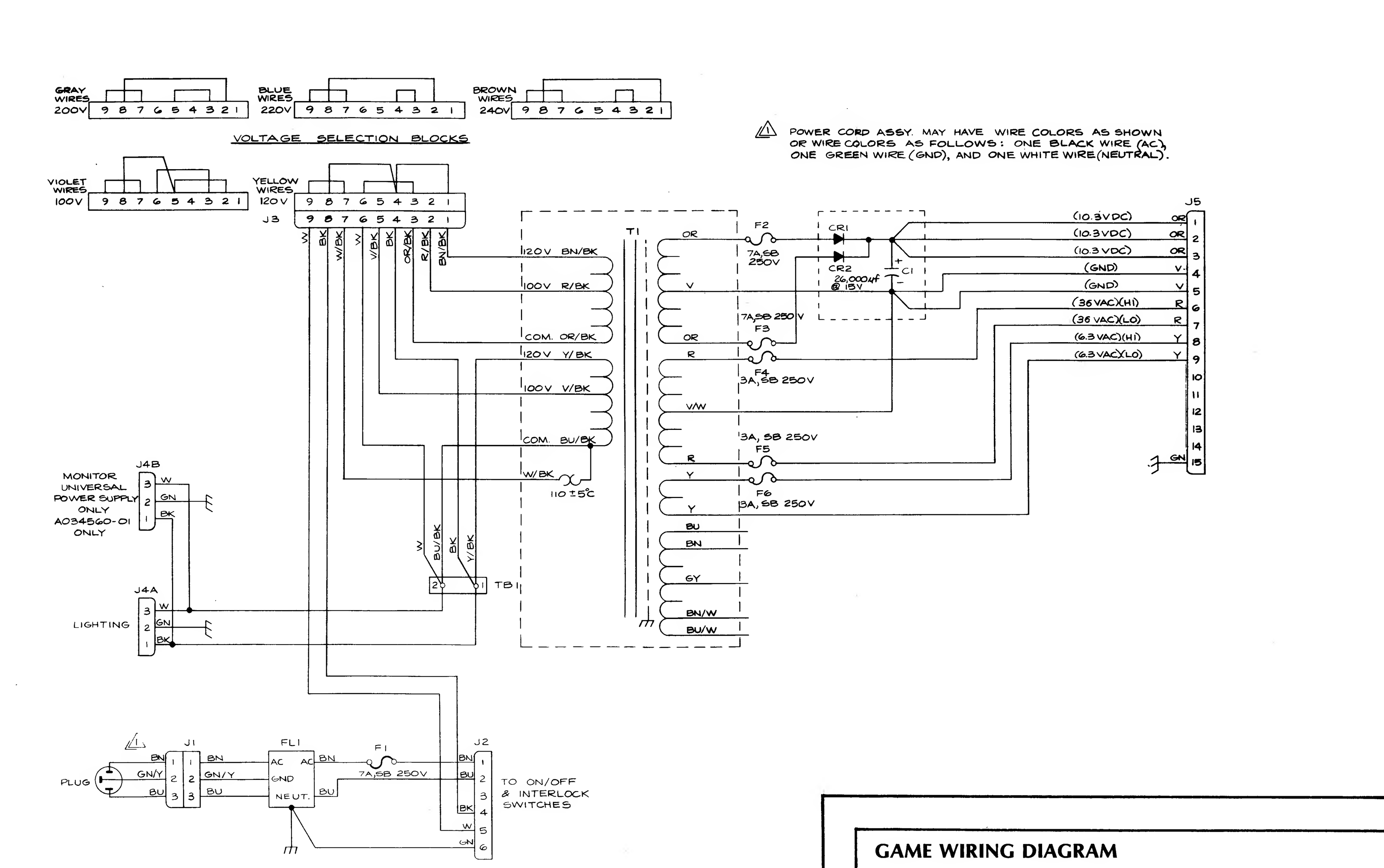
POWER SUPPLY WIRING DIAGRAM (034633-01 A)



REGULATOR/AUDIO PCB SCHEMATIC (034485-01 C)

Regulator/Audio PCB 034485-01 A

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and −SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

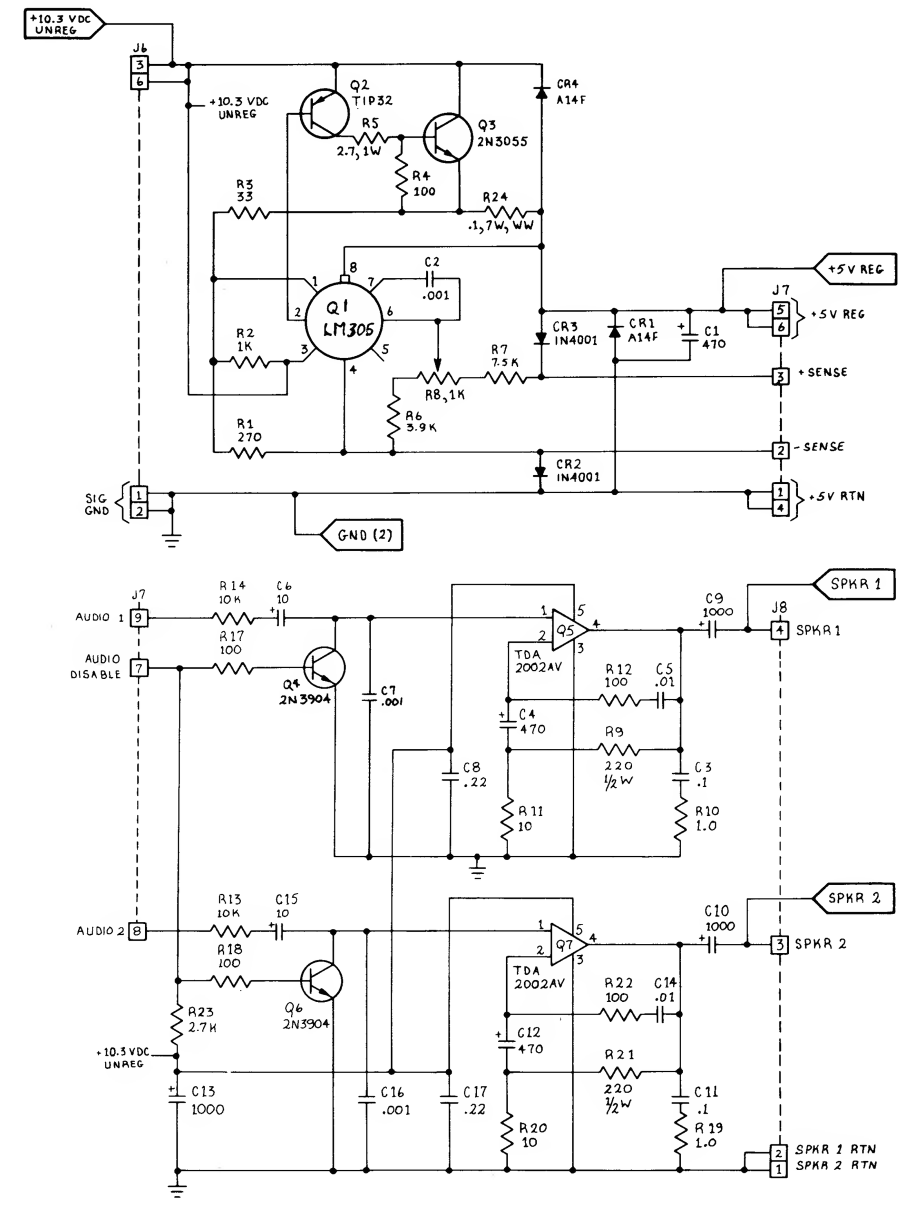
Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

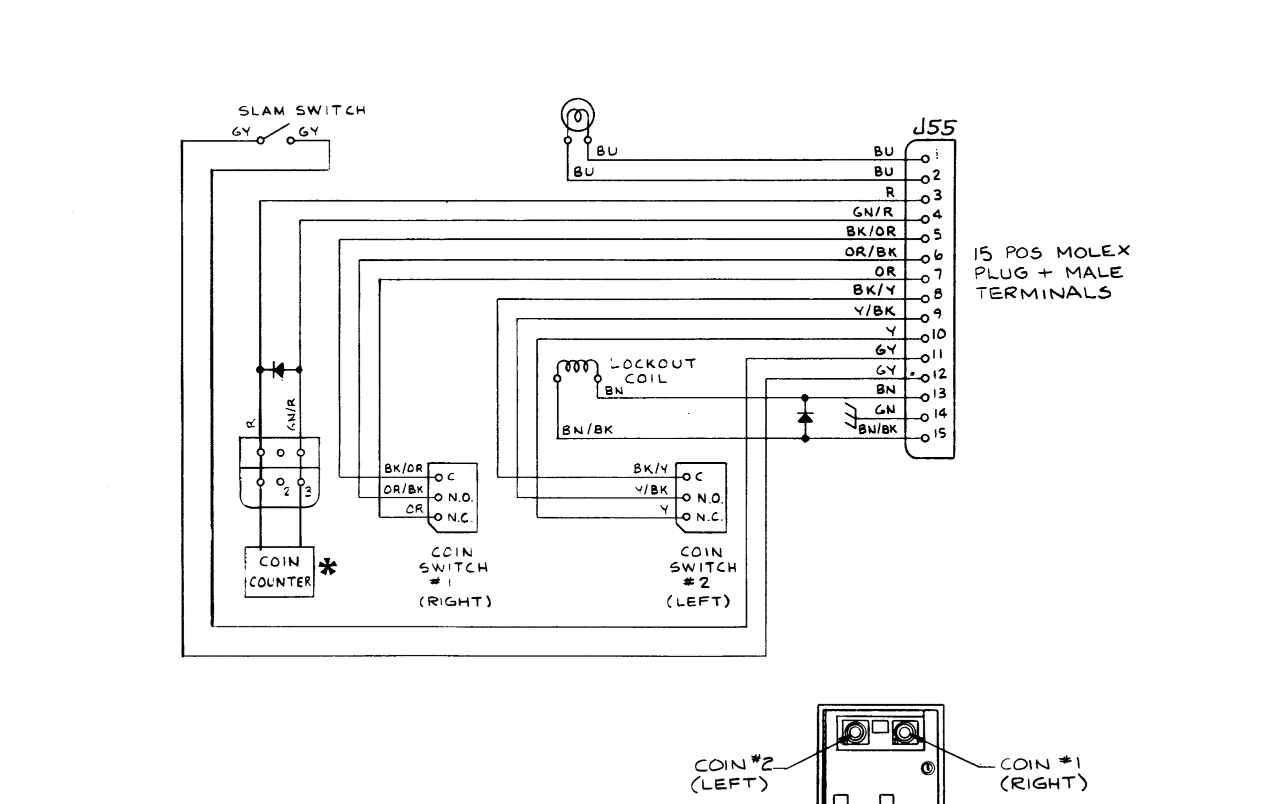
Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten. The AUDIO DISABLE input from the game PCB inhibits both amplifiers from generating any audio during the attract mode.

The audio circuit is repeated on Sheet 1, Side B including more information about its operation.

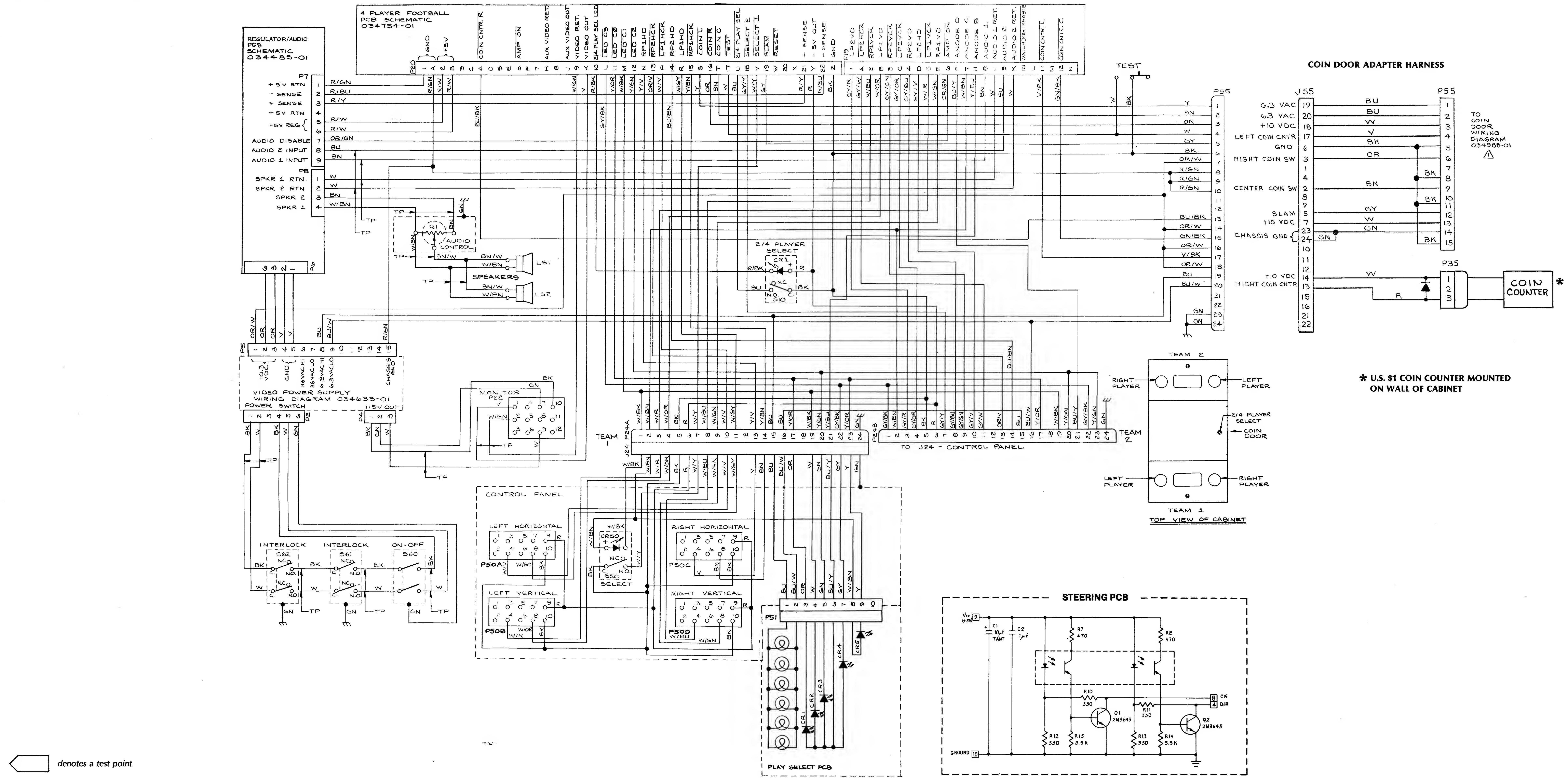


COIN DOOR SCHEMATIC (030401-01 B)



* "Quarter" coin counter mounted on coin door

GAME WIRING DIAGRAM



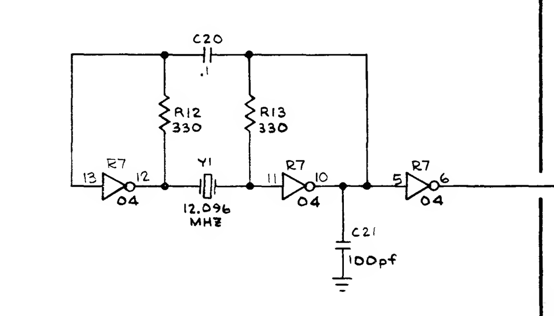
denotes a test point

Drawing Package Supplement to 4-PLAYER FOOTBALL™ Operation, Maintenance, and Service Manual

Contents of this Drawing Package

ATARI®

CLOCK



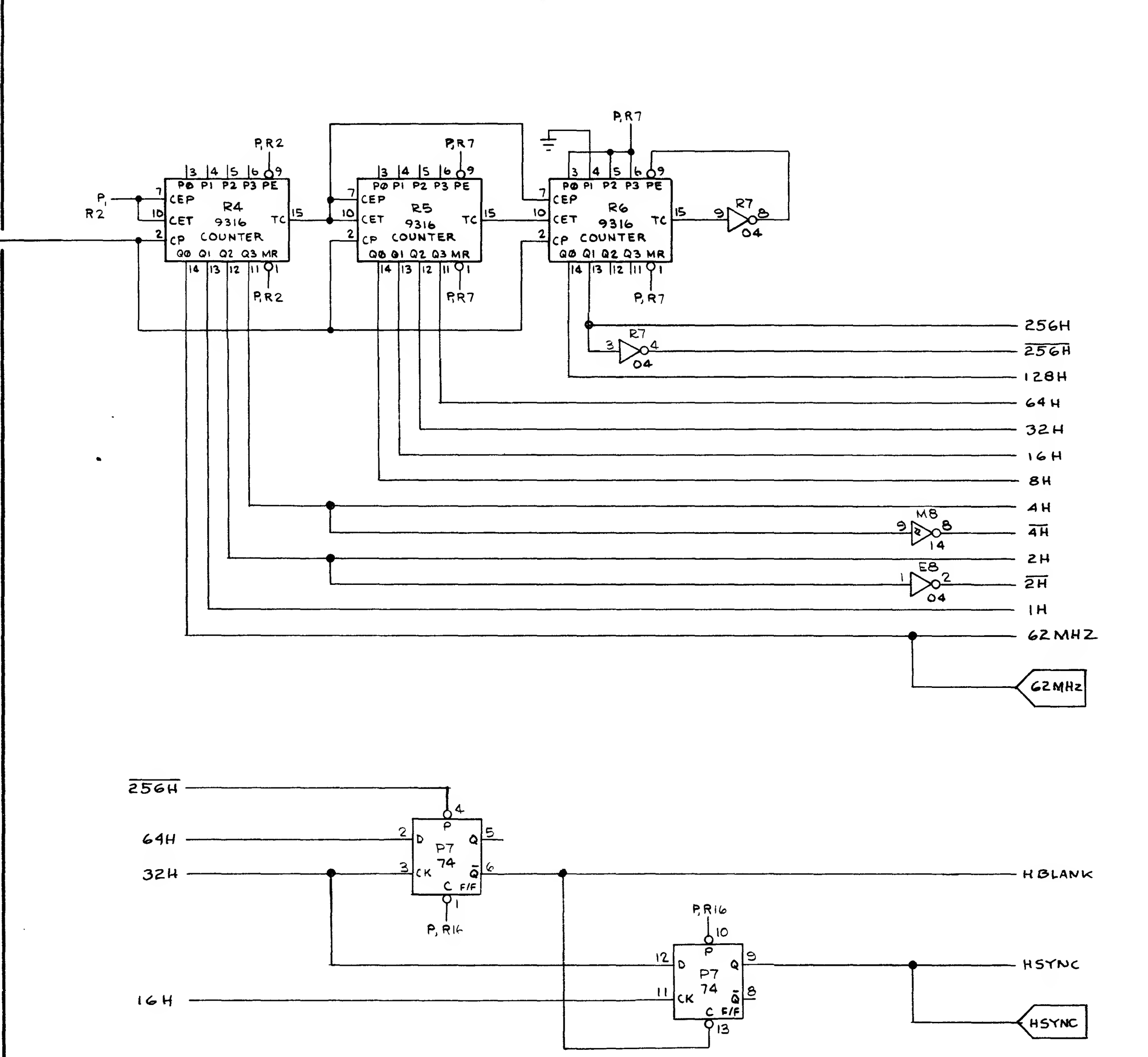
The basic frequency of the sync generator is a 12.096 MHz clock, generated by crystal Y1. The output of the oscillator, viewed with an oscilloscope, is a signal with a period of 83 nanoseconds.

The oscillator frequency is divided down by binary counters R4, R5, and R6. These provide various horizontal synchronization frequencies (1H thru 256H). The final output of the horizontal counting chain is 256H. This signal is, in effect, a division of the oscillator frequency by 768, or 15,750 Hz. The period of 256H is about 63.5 microseconds. The 256H signal, as well as other horizontal signals, are used to generate H BLANK and H SYNC timing pulses.

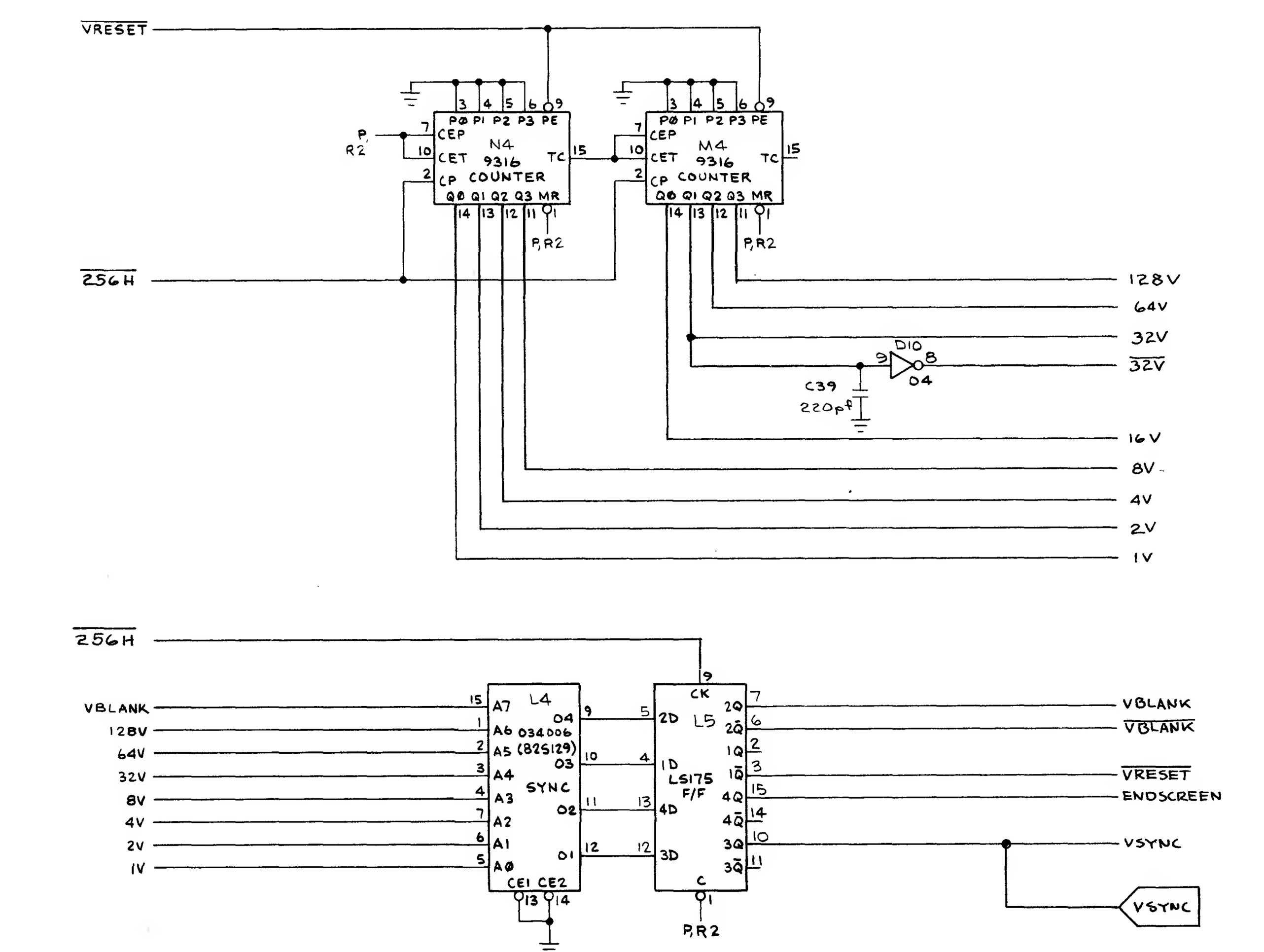
The $\overline{256H}$ signal is used to generate vertical sync signals 1V thru 128V. The 128V signal is, in effect, a division of the $\overline{256H}$ frequency by 262. This results in the final output from the counters of 60 Hz (16.6 milliseconds). The various vertical sync signals address sync PROM L4 whose data is latched at the output of L5.

The end result of the horizontal and vertical timing waveform is to synchronize the TV monitor display. This display consists of 262 horizontal lines per frame: only 240 lines are visible, since the last 22 lines occur during vertical blanking. Each line is equivalent to 768 clock pulses. Each frame is repeated 60 times per second, providing the necessary frequency of display refresh for a stable, non-flickering display.

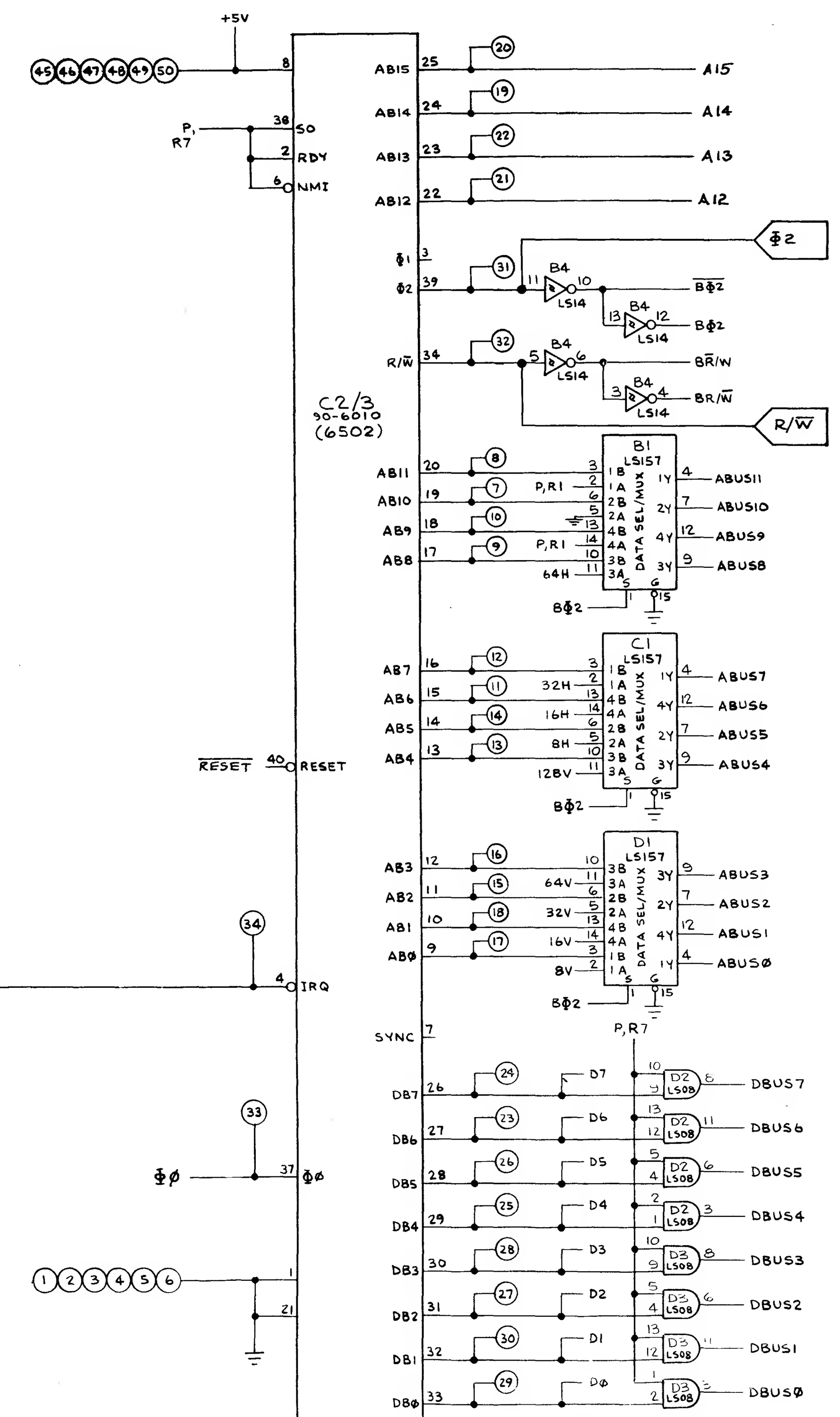
HORIZONTAL SYNC



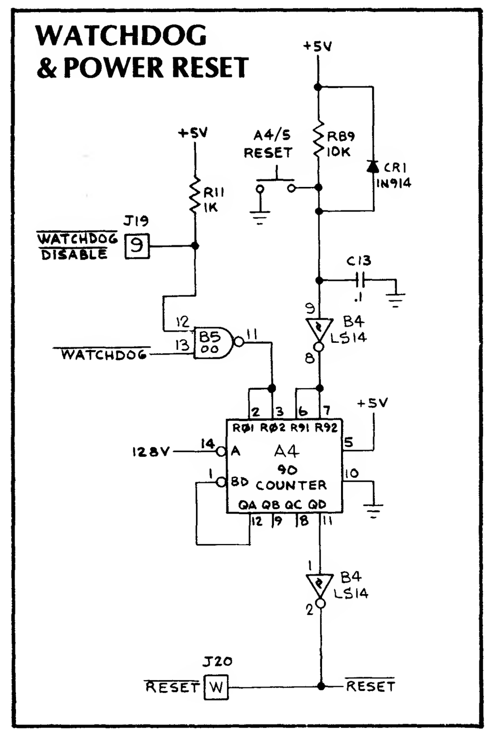
VERTICAL SYNC



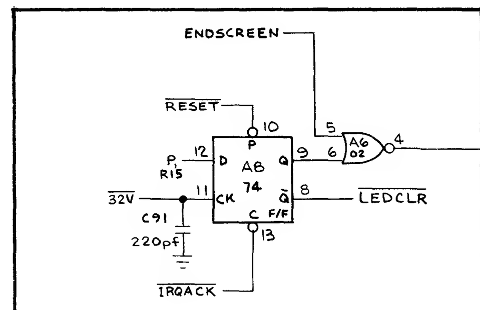
MICROPROCESSOR



WATCHDOG & POWER RESET



INTERRUPT REQUEST



The microprocessor controls all circuits on the game PCB, excluding the Sync Circuit and Watchdog and Power Reset Circuit. The Sync Circuit provides 4H (750 KHz) for the Φ0 clock input to the microprocessor.

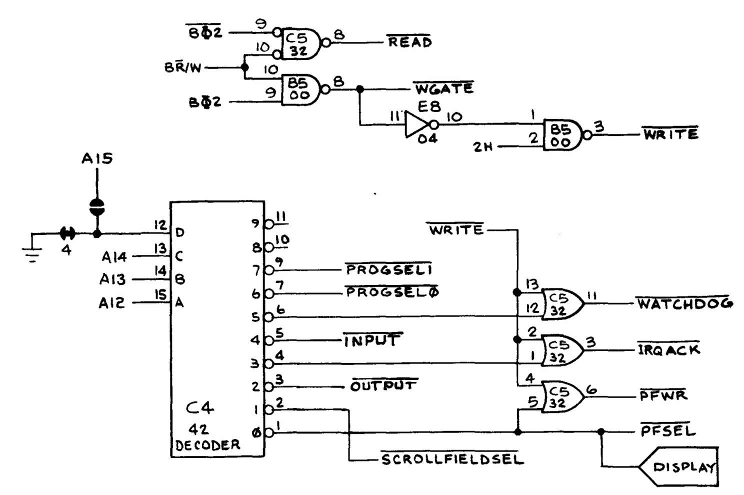
The Watchdog and Power Reset Circuit forces the microprocessor into its initilization sequence during intial power-up, or if the program strays from its normal sequence. When power is initially applied to the PCB, capacitor C13 and resistor R89 form a time constant that forces $\overline{\text{RESET}}$ low until the +5 VDC logic power becomes stable.

During normal operation, the microprocessor outputs address 5000 (hexadecimal) that is decoded by the address decoder for the $\overline{\text{WATCHDOG}}$ signal. This signal is received at the pin 13 input of B5. This signal input causes pins 2 and 3 of counter A4 to go high which resets the counter to a zero count output. If the $\overline{\text{WATCHDOG}}$ pulse is not received before the counter reaches the count of eight, $\overline{\text{RESET}}$ goes low, causing the microprocessor to jump to its initialization sequence.

Flip-flop A8 provides an interrupt request (IRQ) input to the microprocessor. The IRQ is a timing signal used by the microprocessor so it knows when to look for coins, when to write to the LED latches, and when to display motion objects.

Address bus ABUS0 thru ABUS11 is selected from either address lines AB0 thru AB11 from the microprocessor, or from various horizontal and vertical sync signals. This arrangement makes it possible for the microprocessor to write data into or read data out of the RAM when BΦ2 is high. When BΦ2 is low, data is read out of the RAM by the alphanumerics generator.

ADDRESS DECODER



The address decoder receives addresses from the microprocessor, decodes the addresses, and turns on the required circuitry for carrying out the instruction for that address. The address map, to the right of this text, is for the 4-Player Football game. This map provides the necessary information for operating the circuitry with the Atari Automatic ROM/RAM Tester. Before connecting the Tester, do the following:

1. Remove the microprocessor.
2. Short pin 37 to 39 of microprocessor socket C2/3.
3. Ground pin 9 of edge-connector J19.

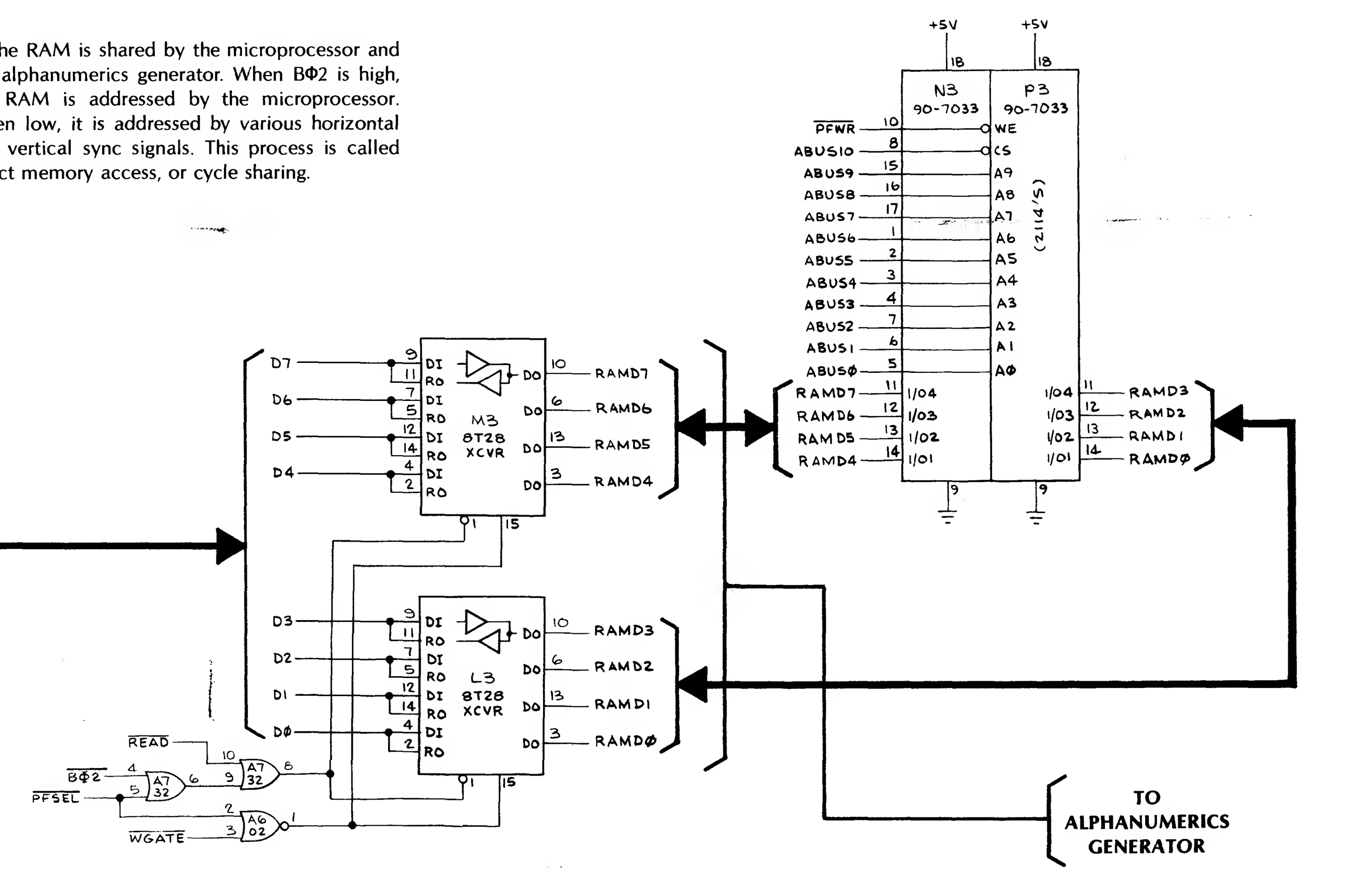
The ones and zeros in the ADDRESS column of the address map indicate the address necessary for information to be passed to and from the microprocessor. A 0 indicates that the address line is low, and a 1 indicates the line is high. Blank spaces indicate that it doesn't matter whether the address line is low or high. An A indicates that the address line is used as part of the functional address for that particular peripheral access. In the DATA column, a D indicates that the data line is used to transfer information.

MEMORY MAP

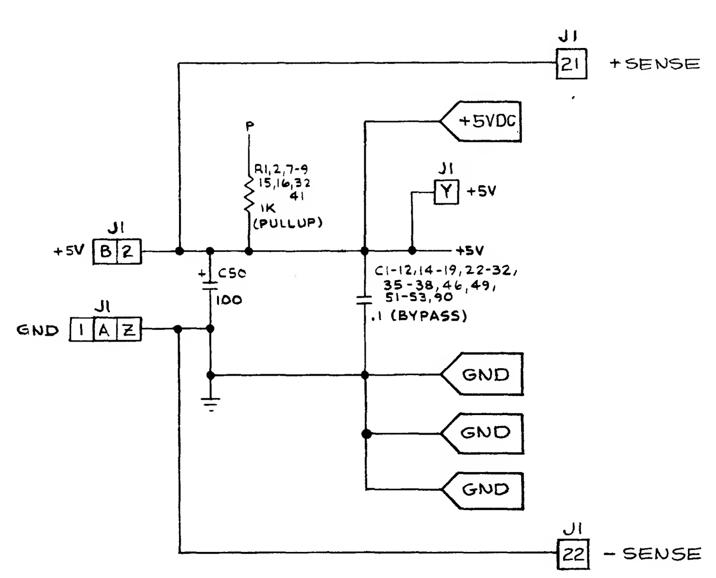
ADDRESS																	R/W	DATA								FUNCTION
HEXIDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0000-07FF	X	Ø	Ø	Ø	X	A	A	A	A	A	A	A	A	A	A	A	X	D	D	D	D	D	D	D	D	0000-02FF WORKING RAM
																										0200-07FF PFLD RAM & MOT OBJECTS
																										MOTION RAM ORGANIZATION
																										13C0 MOT OBJ 1 PIC NO.
																										13C1 MOT OBJ 1 VERT POS
																										13EØ MOT OBJ 1 HORZ POS
																										13E1 SPARE
																										13C2 MOT OBJ 2 PIC NO.
																										13C3 MOT OBJ 2 VERT POS
																										13E2 MOT OBJ 2 HORZ POS
																										13E3 SPARE
																										13DE MOT OBJ 16 PIC NO.
																										13DF MOT OBJ 16 VERT POS
																										13FE MOT OBJ 16 HORZ POS
																										13FF SPARE
1000-13FF	X	Ø	Ø	1	X	X	A	A	A	A	A	A	A	A	A	A	X	D	D	D	D	D	D	D	D	SCROLLFIELD
2000	X	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	Ø	Ø	W	D	D	D	D	D	D	D	D	SCROLLFIELD OFFSET
2001	X	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	Ø	1	W	X	X	X	X	X	X	X	D	WHISTLE SOUND
																		X	X	X	X	X	X	D	X	HIT SOUND
																		X	X	X	X	X	D	X	X	KICKER (RESETS NOISE GEN)
																		X	X	D	X	X	X	X	X	LD1
																		X	D	X	X	X	X	X	X	LD2
																		D	X	X	X	X	X	X	X	COIN CNTR LEFT
2002	X	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	1	Ø	W	X	X	X	X	D	D	D	D	CROWD AMP
																		X	X	X	D	X	X	X	X	COIN CNTR RIGHT
																		X	X	D	X	X	X	X	X	ATTRACT
2003	X	Ø	1	Ø	X	X	X	X	X	X	X	X	X	X	1	1	W	X	X	X	D	D	D	D	D	LED DRIVERS
																		X	X	D	X	X	X	X	X	COIN CNTR CENTER
3000	X	Ø	1	1	X	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X	IRQACK (CLEARS IRQ LATCH)
4000	X	1	Ø	Ø	X	X	X	X	X	X	X	X	X	X	Ø	Ø	R	D	D	D	D	D	D	D	D	(LD1 & LD2 LO) TRACK BALL DIR
																		D	D	D	D	D	D	D	D	(LD1 HI & LD2 LO) RIGHT PLAYER TEAM 1 TRACK BALL CNTRS
																		D	D	D	D	D	D	D	D	(LD1 & LD2 HI) LEFT PLAYER TEAM 1 TRACK BALL CNTRS
4001	X	1	Ø	Ø	X	X	X	X	X	X	X	X	X	X	Ø	1	R	D	X	X	X	X	X	X	X	ENDSCREEN
																		X	D	X	X	X	X	X	X	TEST
																		X	X	X	X	X	D	X	X	COIN3
																								D		COIN2
																									D	COIN1
4002	X	1	Ø	Ø	X	X	X	X	X	X	X	X	X	X	1	Ø	R	D	X	X	X	X	X	X	X	(LD1 & LD2 LO) SEL1 7 4
																		X	D	X	X	X	X	X	X	(LD1 & LD2 LO) SEL2 6 5
																		X	X	D	X	X	X	X	X	(LD1 & LD2 LO) SLAM 5 6
																		X	X	X	D	X	X	X	X	(LD1 & LD2 LO) 2/4 PLY SEL 4 7
																		X	X	X	X	D	D	D	D	DIP SW
																		D	D	D	D	D	D	D	D	(LD1 HI & LD2 LO) RIGHT PLAYER TEAM 2 TRACK BALL CNTRS
																		D	D	D	D	D	D	D	D	(LD1 & LD2 HI) LEFT PLAYER TEAM 2 TRACK BALL CNTRS
5000	X	1	Ø	1	X	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X	WATCHDOG
6000-7FFF	X	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PROGRAM

RANDOM-ACCESS MEMORY

The RAM is shared by the microprocessor and the alphanumerics generator. When BΦ2 is high, the RAM is addressed by the microprocessor. When low, it is addressed by various horizontal and vertical sync signals. This process is called direct memory access, or cycle sharing.



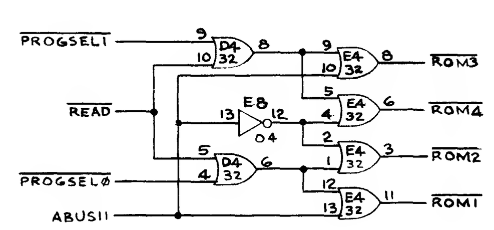
POWER INPUT

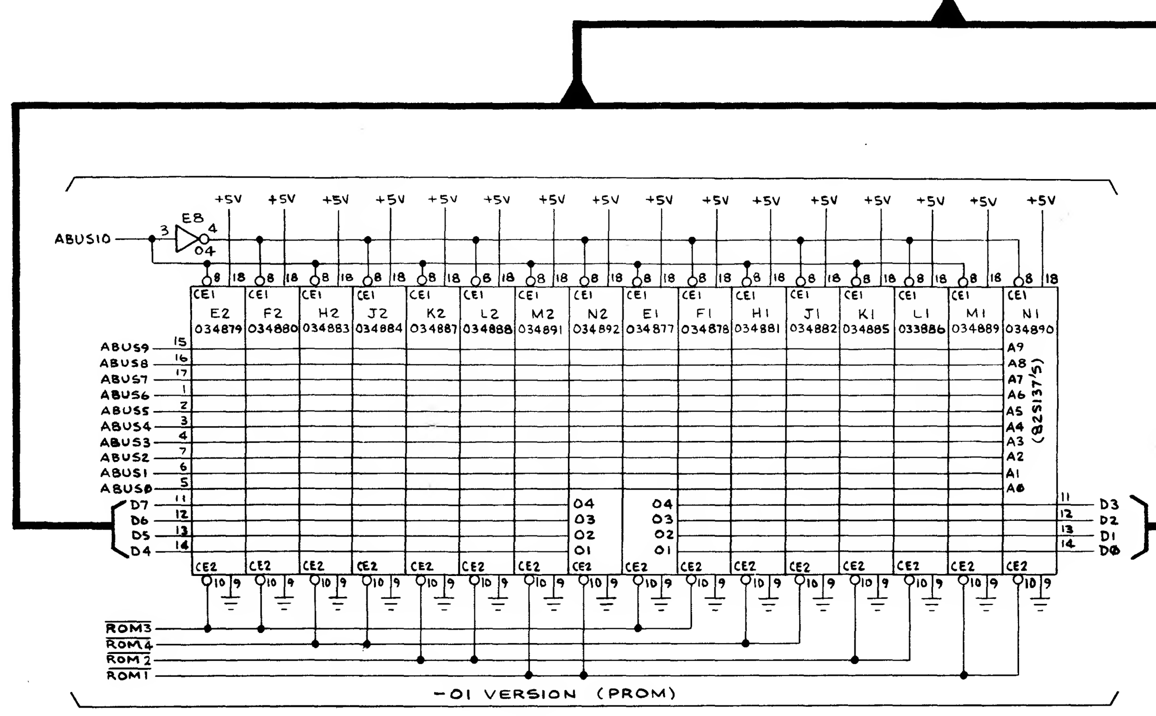


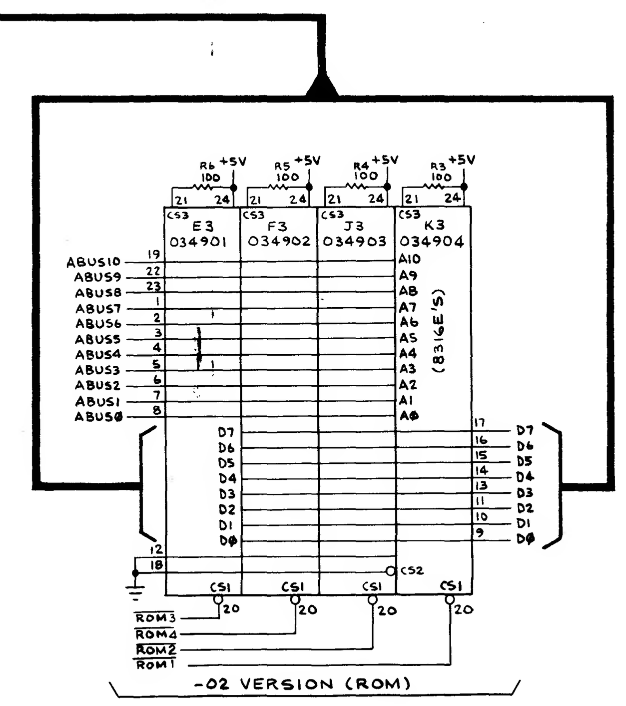
PROGRAM MEMORY

Your 4-Player Football game PCB may contain one of serveral possible program memory chips sets. The -01 version of the PCB contain 16 PROMs for the memory.

The -02 version contains 4 ROM chips for the memory. A third possiblity would be a mixture of ROMs and PROMs. For information regarding which ROMs are equivalent to which PROMs, see the Illustrated Parts Catalog chapter of the game manual.







denotes a test point

4-PLAYER FOOTBALL
MICROCOMPUTER, CLOCK,
SYNC AND MEMORY
034754-xx A

ATARI

VIDEO GENERATOR

The address decoder outputs the scrollfield write enable signal SFWR, and the microprocessor selects the appropriate RAM pair with address lines ABUS0 and ABUS5.

Data Selectors F4, H4, J4 and K4 select the addressing mode for the Video Generator RAM. When 4H is high, the MPU addresses the RAM, via ABUS 0-9. When 4H is low, the Video Generator RAM is addressed by either the scrollfield horizontal address (SFH 3-7) or by the sync chain (8H-64H and 16V-128V). 256H determines which of these two addresses the RAM when 4H is low. When 256H is low sync is selected. When 256H is high, scrollfield is selected.

Multiplexer E6 selects the output of the RAM.

The latched data output of D5 is compared with horizontal sync 8H thru 64H, to enable the playfield to scroll (shift) in steps of 8H. SFH0 thru SFH2 selects the scrollfield output from multiplexer C8 in steps of 1H.

When the RAM is written to by the microprocessor, SFWR is low and a RAM pair is written to by the selection of ABUS0 and ABUS5. Data is written into the RAM through data bus DBUS0 thru DBUS7. Data is read out of the RAM on data lines PFD0 thru PFD31.

The microprocessor reads the latched playfield and motion objects data bytes on data lines D0 thru D7.

Graphics PROMs M5 and N5 contain the graphics data for both the playfield and motion objects. Address inputs PIC0 thru PIC5 select the picture. Inputs GA6 thru GA8 select the actual line of the picture to be output. PIC7 determines whether or not the picture is reflected vertically. PIC6 determines whether or not the picture is reflected horizontally. When MATCH is low, the multiplexers are enabled for writing motion object video data into motion object RAM B6.

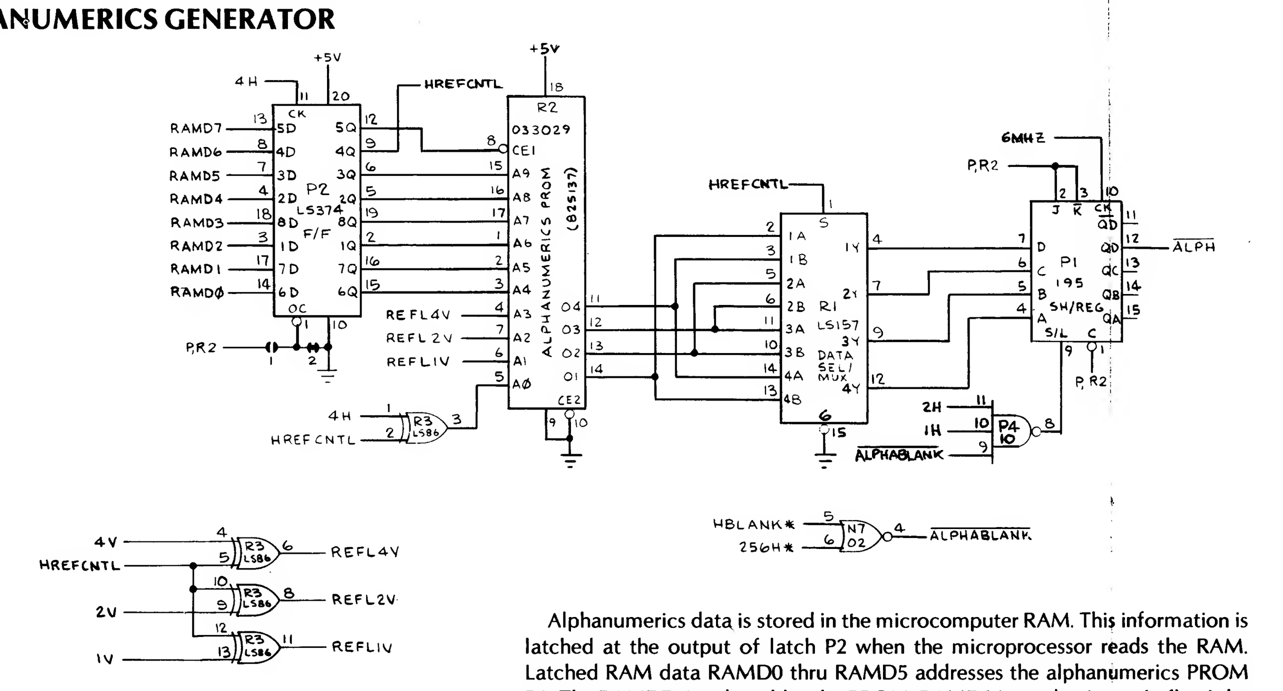
The alphanumerics, playfield, motion objects video and vertical and horizontal sync signals are all summed at the video summer. The VBLANK signal ensures that there is no video during the vertical blanking period.

The SCROLLGATE signal ensures that the playfield and motion object video is only output during the portion of the screen scanned, when 256H is high, conditioned by 256H**.

Adders H8 and K8 compare the vertical line presently being scanned with RAM data PFD8 thru PFD15, which define the vertical location of the motion object. When the inputs are equal, MATCH is latched low, permitting the motion object data to be output from the graphics PROM. LINE0 thru LINE2 count up for the eight scan lines of the motion object picture.

Motion object video is written into RAM B6 during horizontal blanking. Signals PFD16 thru PFD23 latched at the output of D7 define the horizontal location of the motion object on the scan line. When HLD goes low, the position data is loaded into counters B7 and C7. The output of counters B7 and C7 then are used to address RAM B6, so that RAWVID picture data can be loaded into the RAM. At the beginning of the actual scan line, counters B7 and C7 are reset to zero. The output of counters B7 and C7 are clocked up at a 6-MHz rate. When they reach the address at which the motion object video was loaded into the RAM for that particular scan line, the video data is outputted from RAM B6, and sent to the video summing circuit (A8, pin 2).

ALPHANUMERICS GENERATOR

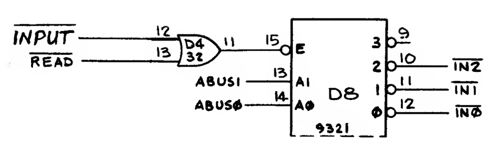


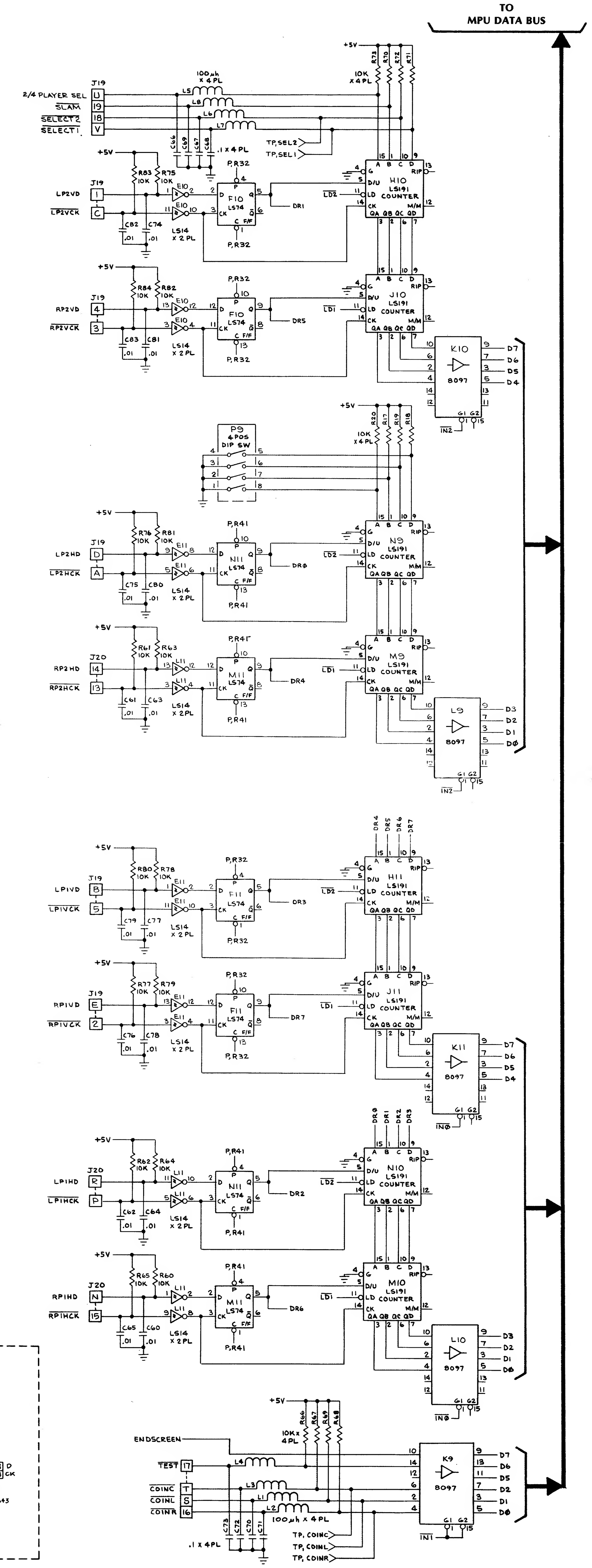
Alphanumerics data is stored in the microcomputer RAM. This information is latched at the output of latch P2 when the microprocessor reads the RAM. Latched RAM data RAMD0 thru RAMD5 addresses the alphanumerics PROM R2. The RAMD7 signal enables the PROM. RAMD6 is used to invert (reflect) the data output of the PROM both horizontally and vertically at the output of multiplexer R1. Therefore, the same data output is used at both ends of the monitor. The ALPHABLANK signal ensures that the alphanumerics appear only at each end of the horizontal scan line.

ATARI

**4-PLAYER FOOTBALL
VIDEO GENERATOR AND
ALPHANUMERICS GENERATOR
034754-xx A**

SWITCH AND TRAK BALL INPUTS

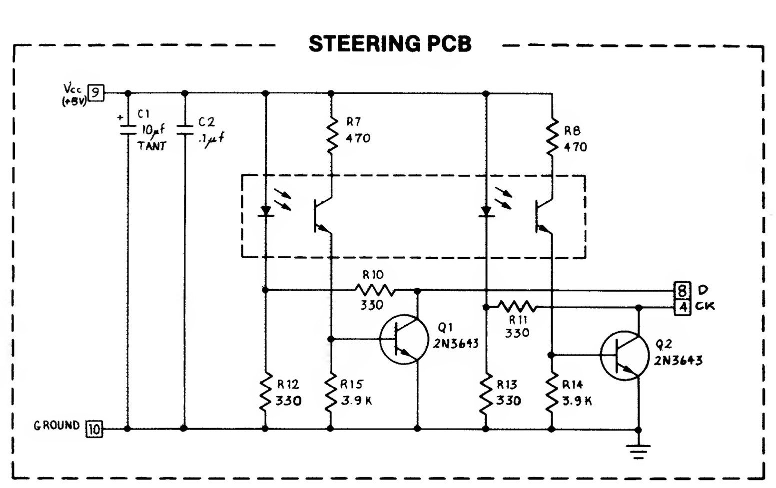


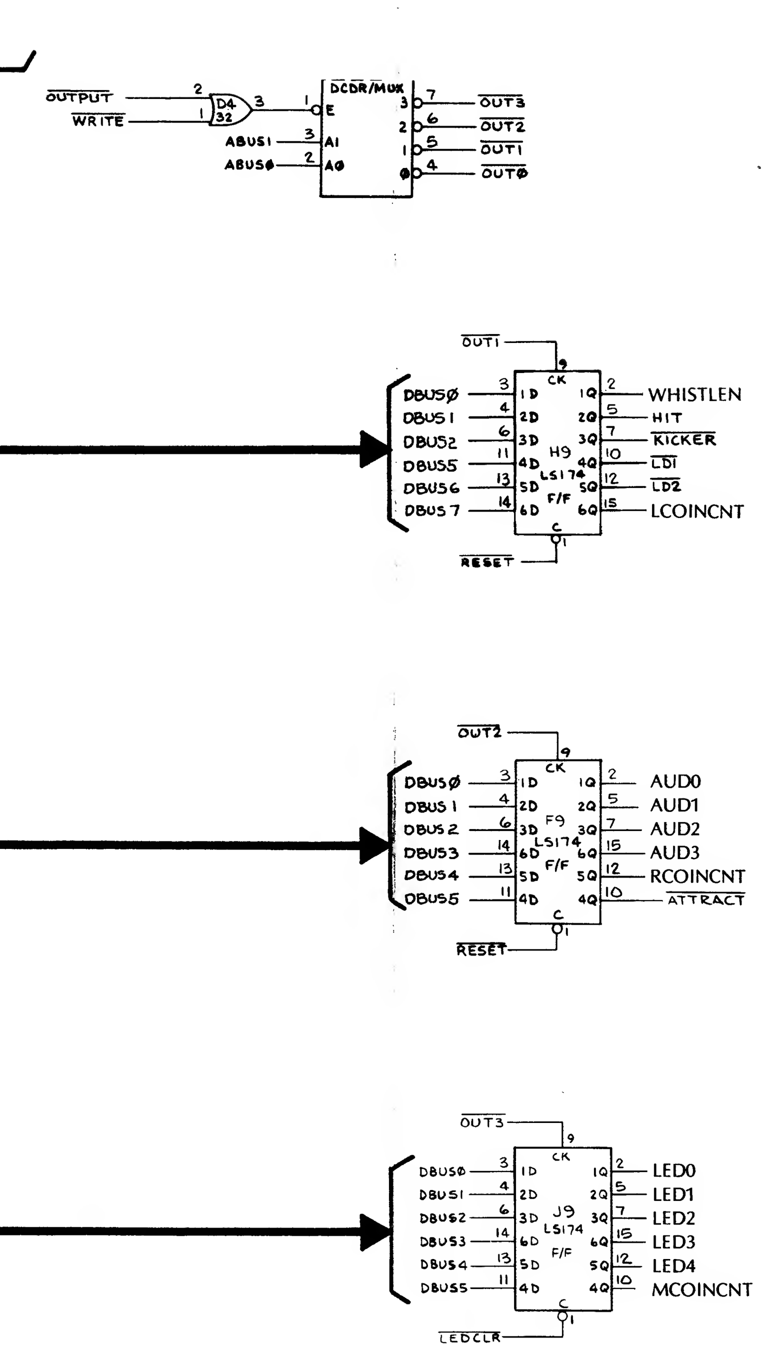


The sequence for reading the $\overline{\text{SELECT1}}$, $\overline{\text{SELECT2}}$, $\overline{\text{SLAM}}$, $\overline{\text{2/4PLAYER}}$, and option switches is as follows:

1. $\overline{\text{LD1}}$ and $\overline{\text{LD2}}$ are latched low at the output of H9 on the rising edge of $\overline{\text{OUT1}}$.
2. $\overline{\text{IN2}}$ from the address decoder enables input ports L9 and K10.
3. The microprocessor reads the switches on data lines D0 to D7 through counters M9, N9, H10 and J10.

The Trak Balls are read by the microprocessor through input ports L9, L10, K10 and K11. Ports L9 and K10 are enabled by $\overline{\text{IN2}}$ from the address decoder, and L10 and K11 are enabled by $\overline{\text{IN0}}$. When $\overline{\text{LD1}}$ and $\overline{\text{LD2}}$ are both high, the microprocessor reads the rate of turn for the Trak Balls connected to J11 and M10, or connected to J10 and M9. When $\overline{\text{LD1}}$ is low and $\overline{\text{LD2}}$ is high, the microprocessor reads the rate of turn for the Trak Balls connected to the input of counters H11 and N10, or H10 and N9. When $\overline{\text{LD1}}$ and $\overline{\text{LD2}}$ are both low, the microprocessor reads the direction of the "right hand" Trak Balls on data lines D4-D7, and the "left hand" Trak Balls on data lines D0-D3.





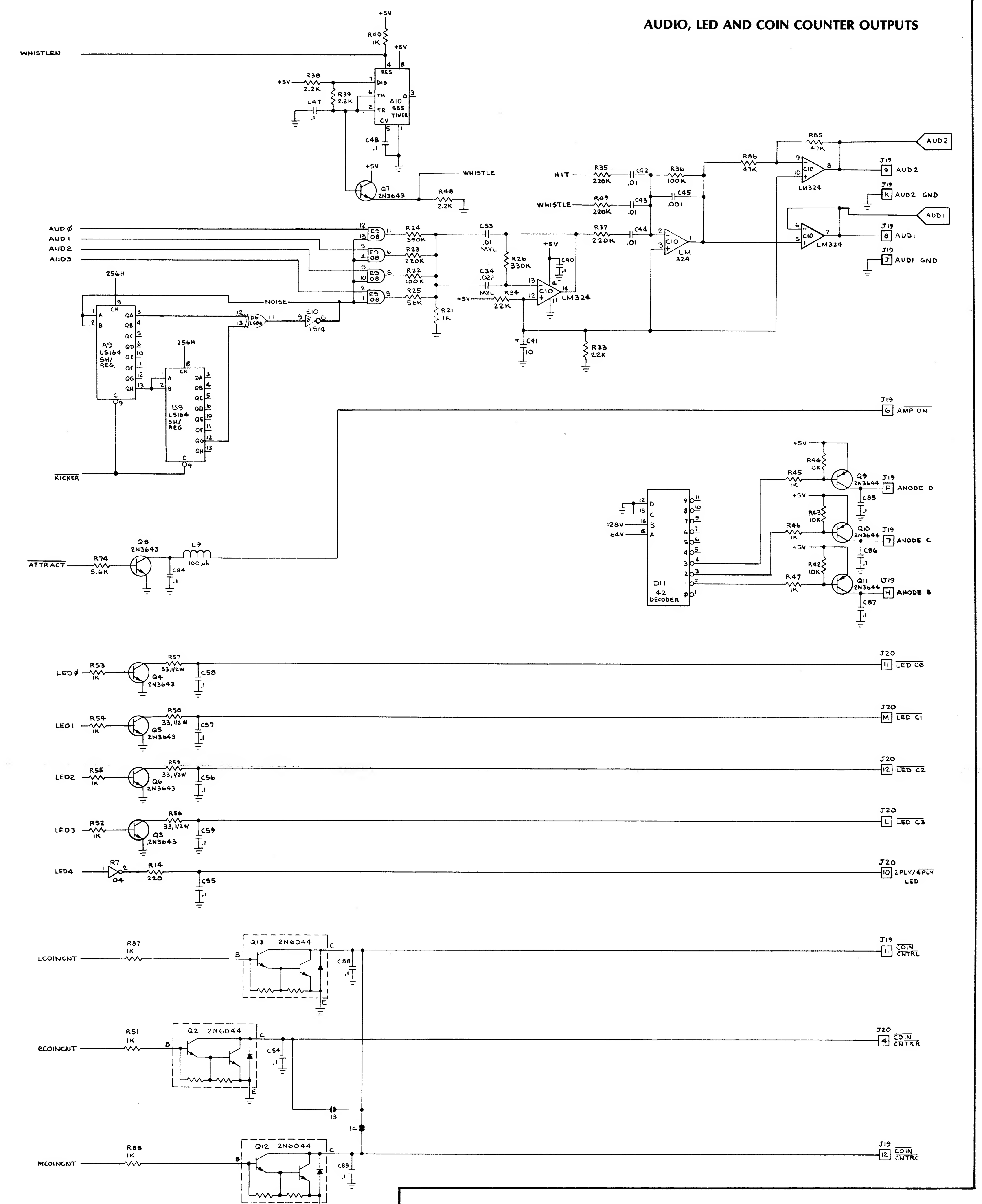
The audio generator generates the crowd, hit, and whisle sounds. The crowd sound is generated from random noise from A9 and B9. The volume of the crowd sound is controlled the AUD0 thru AUD3 data latched at the output of F9. Hit is enabled by the HIT data latched at the output of H9. (A "hit" occurs when the ball is caught or kicked.)

Whistle is enabled by WHISTLEN data from the output of latch H9. The audio output to the Regulator/Audio PCB is out of phase at the J19 connector, pins 8 and 9. Therefore, the audio section of the Regulator/Audio PCB acts as a push-pull amplifier. The amplifier is enabled when $\overline{\text{ATTRACT}}$, from latch F9, is high.

The LEDs on the top of the 4-Player Football game are connected in a matrix. The anodes are strobed by vertical sync. The cathodes are controlled by latched data from the microcomputer. The $\overline{\text{LEDCL}}$ signal is generated by the IRQ counter at the IRQ input of the microprocessor. Since the microprocessor knows when each LED anode driver is being strobed at any given time, all the microprocessor needs to do to light an LED is latch the appropriate data line by outputting the address for the $\overline{\text{OUT3}}$ enabling signal from the address decoder. When the latched data line is high, the appropriate LED is lighted. Team 1 LEDs, excluding their kick LED, are connected to anode B. All Team 2 LEDs, excluding their kick LED, are connected to anode D. The kick LEDs of both Team 1 and Team 2 are connected to anode C.

Coin and self-test switch inputs are connected to +5 VDC through pullup resistors. When a switch is closed, that input is pulled to ground. The switch is read by the microprocessor when switch input port K9 is enabled by $\overline{\text{IN1}}$ from the address decoder.

AUDIO, LED AND COIN COUNTER OUTPUTS



denotes a test point

4-PLAYER FOOTBALL
SWITCH INPUTS, COIN COUNTER
AND LED OUTPUTS
034754-xx A

ATARI®

DP-139-02 1st PRINTING